Future Concepts for On-board Timing Subsystems for Navigation Satellites

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ABSTRACT

All signal generation and transmission frequencies in the payload of a navigation satellite are typically derived from a single 10.23 MHz master clock. In case of the current payload architecture of the Galileo or other Navigation System this Master Timing Reference (MTR) is synthesized in a Clock Monitoring and Control Unit (CMCU) based on one single atomic reference. To achieve this, in the current Galileo design the CMCU selects the active clock from a pool of two Rubidium Atomic Frequency Standards (RAFS) and two Passive H-Masers (PHM) and synthesizes the MTR from this source. A second atomic clock is kept in hot redundancy and monitored inside the CMCU for its phase drift against the active clock.
However this concept does not provide any protection against misbehaviour of the sole active clock in case of unexpected high frequency drifts or frequency jumps. For this reason future concepts are under investigation at Astrium to derive the MTR simultaneously from multiple atomic clocks by composite clock methods supported by frequency jump detection algorithms.
This paper describes the hardware concepts for current CMCUs as well as a next generation CMCU based on composite clock techniques including the multi-channel phase comparison system to provide the input source for the algorithms and the frequency synthesis to generate the MTR output frequency.

INTRODUCTION

As shown in Figure 1 the payload of the Galileo navigation satellite consists of a clock ensemble with two Passive H-Masers (PHM) and two Rubidium Atomic Frequency Sources (RAFS) that provide the time reference for the generation of the navigation signal. The atomic reference is selected and converted to the Master Timing Reference (MTR) of 10.23 MHz by the Clock Monitoring and Control Unit (CMCU).

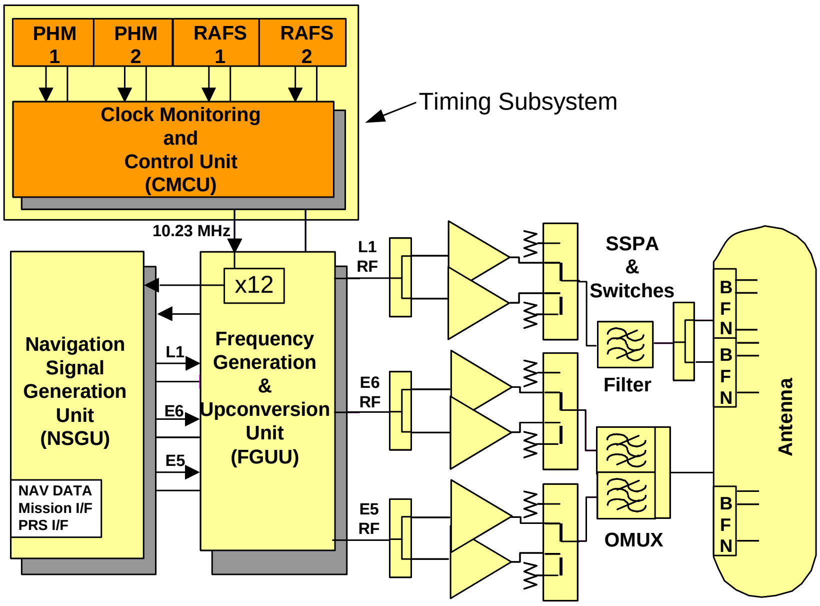

Figure 1. Timing Subsystem embedded in the Galileo Payload.

The MTR provides the reference for the Frequency Generation and Up-conversion Unit (FGUU) to generate the master clock for the Navigation Signal Generation Unit (NSGU) and up-convert the navigation signals to their transmission frequencies.
The CMCU synthesizes the MTR on the selection of one out of the four Atomic Frequency Standards (AFS) as depicted in the block diagram in Figure 2 for the currently established CMCU concept. The input switch matrix selects two out of the four atomic clock signals by telecommand and provides each of them to an individual synthesizer. The output signal of one synthesizer is selected by telecommand to become the MTR to be provided to the remaining payload.
To keep the AFS untouched while adjusting the MTR to system needs, the synthesizers are tunable in frequency steps of less than 1e-15 over a frequency range of 1e-8. These hyperfine tuning steps are achieved by Direct Digital Synthesizers (DDS) generating internal auxiliary frequencies that are tuneable with the required fine granularity. To overcome the spurious problems with conventional DDS circuits new noise shaping technologies are applied as already presented in [2].
To gain knowledge on the frequency characteristics of the second clock running in hot redundancy in the background, a phase meter compares the selected MTR against the output signal of the second synthesizer. In the Galileo payload a frequency offset of approx. 2.8 kHz exists between the PHM and the RAFS. For this reason the phase comparison is only possible after the frequency conversion that is conducted with two different synthesizers.

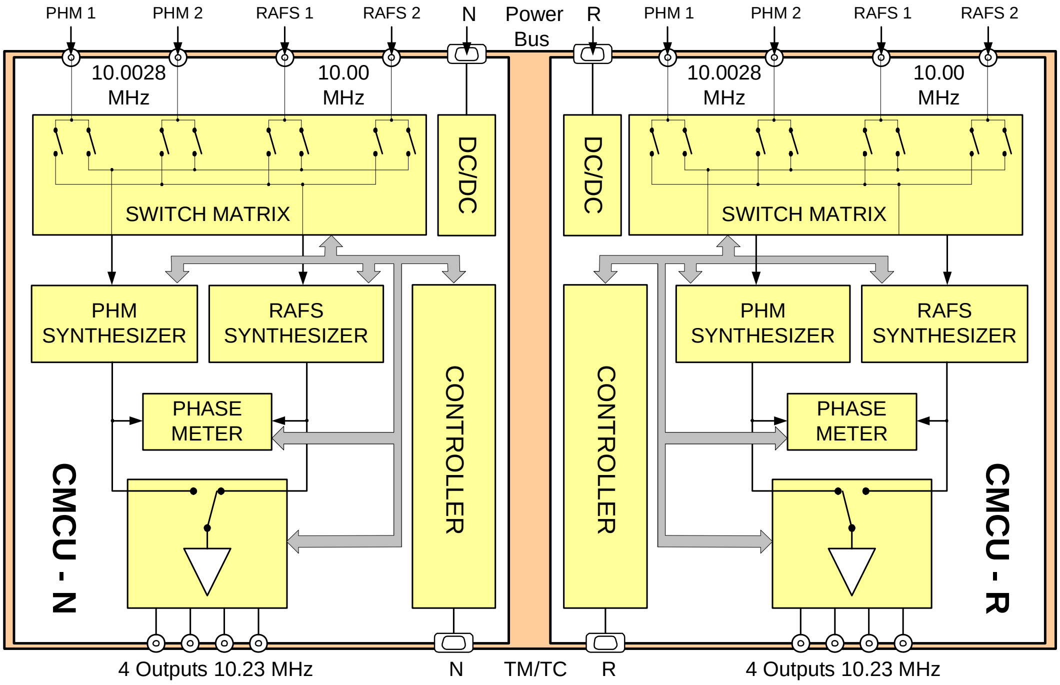

Figure 2. Block Diagram of a Galileo IOV-like CMCU.

DISCUSSION OF CRITICAL PERFORMANCE PARAMETERS

To maintain the signal performance of the selected atomic references in terms of stability and spectral purity, isolation inside the CMCU as well as the system concept of the synthesizer are key requirements. By adapting the synthesizer to the characteristics of the input clock, the MTR may provide an even superior short term performance compared to the clock signal.

Isolation between Signals

The stability of the atomic clock signal can be easily degraded by cross-coupling between different clock signals in the input stage of the CMCU. In order to derive requirements for the maximum tolerable leakage into the wanted signal, the maximum phase distortion is determined. Figure 3 shows the rotating vector of the wanted signal in the complex domain and its superposition by the cross-coupling from an adjacent input and the resulting maximum phase error.

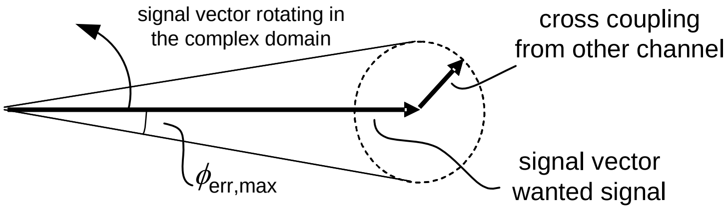

Figure 3. Wanted and unwanted signal components rotating in the complex domain.

The worst case is given by a vector of the cross coupling signal perpendicular to the wanted signal and showing a phase rotation of e.g. 180° between two subsequent phase measurements. With these assumptions inserted into the equation for the Allan Deviation [3] the relation between cross-coupling and degradation of stability can be determined.

$$\sigma_y = \sqrt{\frac{1}{2(N-2)\omega_0^2\tau^2}\sum_{i=1}^{N-2}\left(\varphi(i+2)-2\varphi(i+1)+\varphi(i)\right)^2}$$

$$\sigma_y = \frac{\sqrt{8}\cdot\varphi_{\text{err,max}}}{\omega_0\tau} \quad \Rightarrow \quad \sigma_y\frac{\omega_0\tau}{\sqrt{8}} = \varphi_{\text{err,max}} \approx \text{Cross Coupling}$$

Inserting the short term stability of 1e-12 for intervals of 1 second as specified to the PHM into this equation leads to an isolation of more than 93 dB to be obeyed for limiting the worst case distortion to the magnitude of the specified clock stability. This analysis is also valid for cross-coupling between the output signals of the two synthesizers, if a CMCU system design as shown in Figure 2 is envisaged.

Injection Locking of Atomic Clocks

The second effect that could degrade the clock stability could be caused by injection locking between the different clocks due to limited isolation. Adler's equation [4] describes, how a resonant circuit can be affected by injecting a frequency close to its resonance dependent on the injected current I_i related to the current inside the resonator I_r, the offset frequency and the quality factor Q of the resonator.

$$\frac{d\Delta\varphi}{dt} = \Delta f_0 - \frac{I_i}{I_r}\cdot\frac{f_0}{2Q}\cdot\sin\left(2\pi\Delta\varphi(t)\right) \quad \text{(=0 if injection locking occurs)}$$

$$\underbrace{\frac{\Delta f_0}{f_0}}_{\text{Rel. Freq. Offset}} \cdot 2 \underbrace{Q}_{\text{Resonator Quality Factor}} = \underbrace{\frac{I_i}{I_r}}_{\text{Rel. Magnitude of Distortion}}$$

As sketched in Figure 4 the typical isolation can be expected to be in the order of 150 dB if the backward isolation of the buffer amplifiers inside the atomic clock is taken into consideration which reduces the cross-coupled signal to levels below the phase noise curve of the wanted signal. For this reason injection locking is not assumed as a source of degradation if the isolation requirements as discussed in the previous paragraph are obeyed.

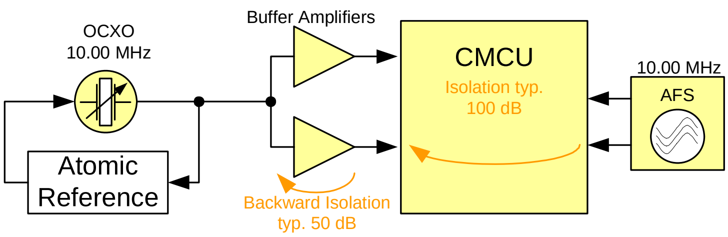

Figure 4. Isolation between the output signal of the output signal and the resonator of two adjacent atomic clocks.

Distortions inside the Frequency Synthesizer

As already presented in greater detail in [2], the synthesizers are based on a hybrid PLL steering the frequency difference between input and output signal to an auxiliary frequency generated by a Direct Digital Synthesizer (DDS). Due to the DDS the hyperfine frequency increments become possible that are needed to correct for the frequency offset of the atomic clocks. The major drawback of DDS circuits is their tendency to generate spurious dependent on the programmed frequency control word very close to the wanted signal. Although the PLL loop filter with a bandwidth of less than 1 Hz is very small, the spurious could pass the PLL and degrade the output signal, if close enough to the carrier frequency.

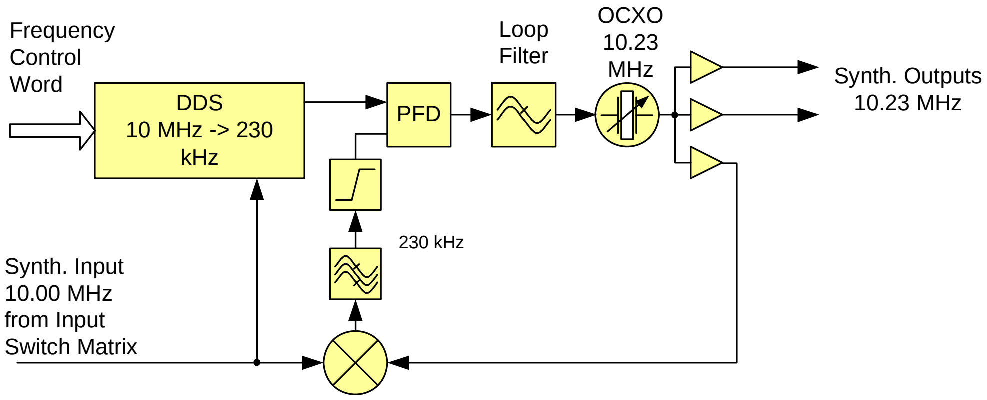

Figure 5. PLL concept of the CMCU Synthesizer.

To prevent these effects, a noise shaping was integrated inside the DDS, shifting the energy of the spurious signals to the higher frequency ranges where they can easily be filtered out by the loop filter of the PLL.

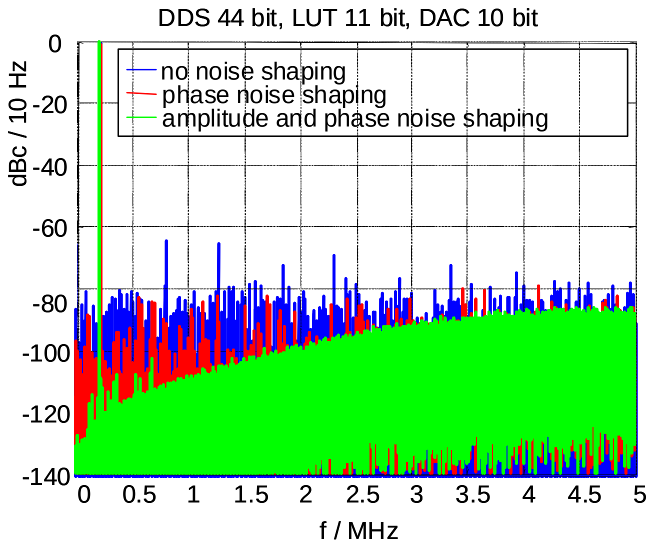

Figure 6. Spectral improvements by noise shaping inside the DDS.

Phase Meter

Although beside parasitic effects like cross-coupling inside the phase meter or leakage of the local oscillator signal, the phase meter has no impact on the performance of the output signal a short description shall be given here for the sake of completeness in describing all major CMCU building blocks.

The phase meter concept as depicted in Figure 7 is based on the Dual Mixer Time Difference (DMTD) concept [3] with the modification, that the auxiliary frequency as necessary for the homodyne down-conversion is locked to one input signal. By doing this, the range of the interval counter is mapped to 360° phase difference between the two signals. A range of 15 bits provides a resolution of 3 ps for a single measurement which is already less than the specified performance of the RAFS (5e-12 $\tau^{-1/2}$) for 1 second intervals. As the phase measurements are to be conducted in programmable intervals, potential multiple phase wraps between two consecutive measurements need to be resolved. For this reason an up-/down counter is implemented which reflects the difference between in phase wraps on the two input signals between two measurements.

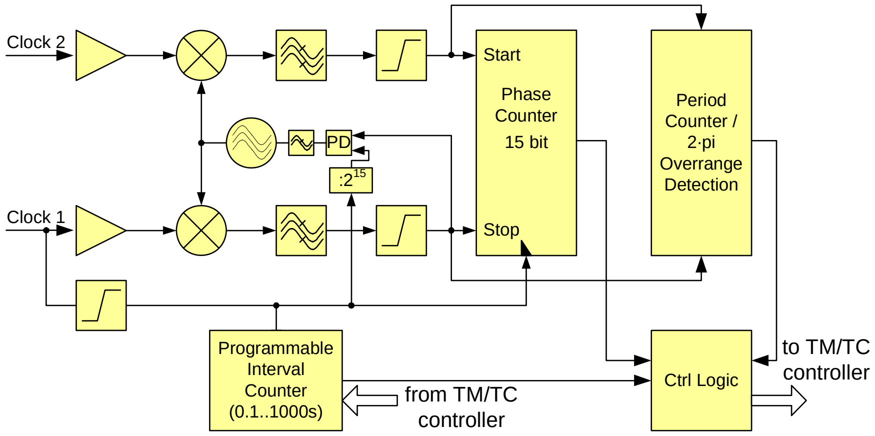

Figure 7. Block Diagram of the Phase Meter.

FURTHER CURRENT CMCU CONCEPT

The descriptions as given previously were based on the initial CMCU concept for Galileo as shown in Figure 2. This concept was realized by Astrium on Engineering Model level on internal funding. It is not part of the current GALILEO IOV payload.
In 2008 Astrium got the contract for the delivery of 9 Flight Models of a timing subsystem consisting of 3 RAFS (SpectraTime) and a CMCU modified to customer preferences. This system is depicted in Figure 8.

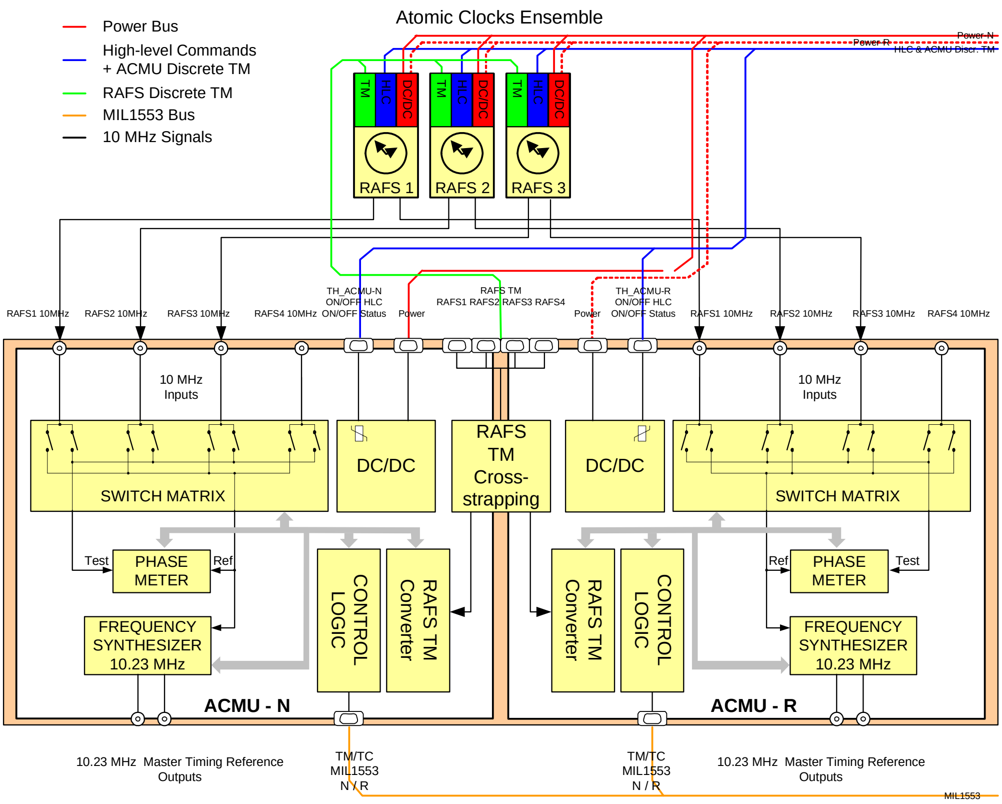

Figure 8. Timing Subsystem with three RAFS and CMCU , collecting RAFS telemetry offering a MIL-1553 Interface.

Also in this concept one clock is taken as a reference to provide the MTR and a second clock is kept in hot redundancy monitored by the phase meter. As all three clocks are operating on the same frequency, the phase comparison can be preformed at the input frequency and the second synthesizer becomes superfluous. Another advantage of this concept is the collection of clock discrete telemetry data by a mini-RTU implemented into the CMCU. The data can be retrieved via a MIL-1553 interface. Beside potential operational benefits when the satellite is in safe mode, this idea provides a reduction in harness mass. Synthesizer and phase meter concepts are identical to the ones described previously.

ADVANCED CONCEPT FOR GALILEO FOC

Based on the described experience, Astrium has developed an advanced CMCU concept for the Galileo FOC phase as shown below. One of the key drivers for developing this concept was to maximize the isolation between the different signal inputs. To achieve this, the input switch matrix at RF frequencies was eliminated by providing a separate down-conversion to each channel. On the output side, the presence of two 10.23 MHz signals was avoided by removing one synthesizer loop. The operation of the phase meter even in presence of different input frequencies of RAFS and PHM was enabled by introducing a second down-conversion with an auxiliary frequency with different DDS modules for RAFS and PHM compensating this frequency offset. The synthesizer loop of this concept was already experimentally verified on breadboard level providing similar results as the previous CMCU concept.

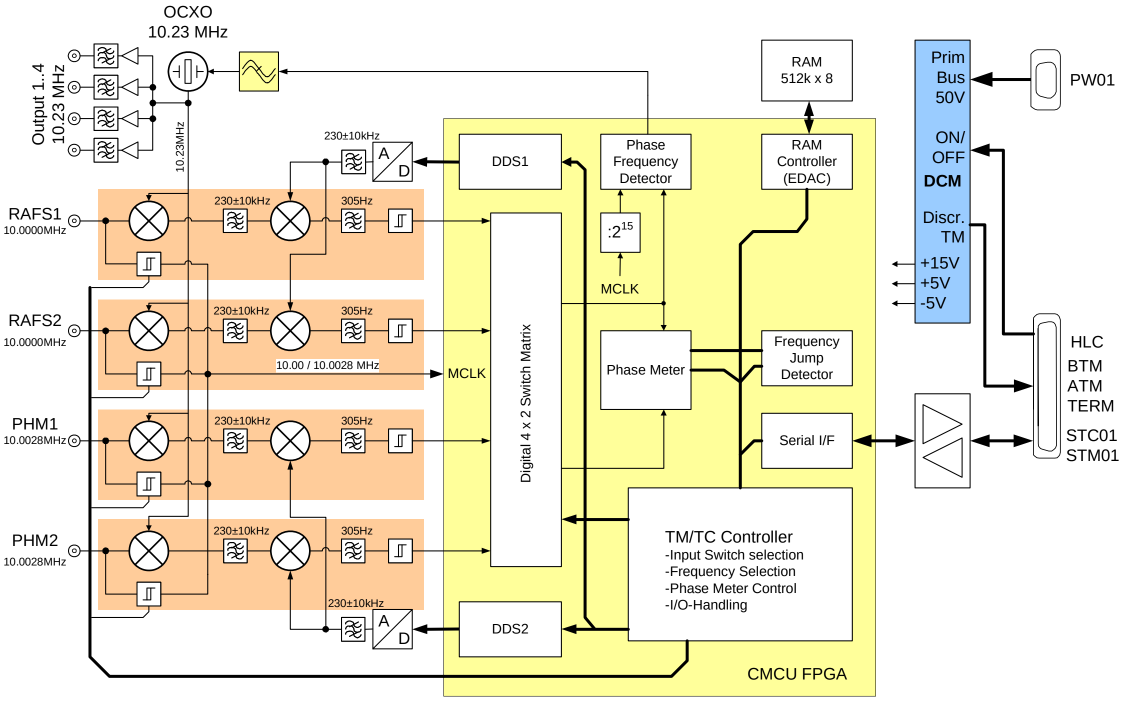

Figure 9. Advanced CMCU Concept for Galileo FOC.

FUTURE EVOLUTION TRENDS

According to current study results [5] it seems to be very likely, that future timing subsystems will remain autonomous on each satellite (e.g. no inter-satellite links to establish a clock for the whole constellation) but may be based on composite clock techniques. The major motivations behind this are the removal of the dependency of the output signal from one single clock in case of its failure (excessive drift, frequency jumps) and to find an over-all optimum compromise between clock cost, weight, power consumption, lifetime and performance of the CMCU output signal. E.g. a simplified comparison between the current RAFS and PHM shows, that the PHM provides a 5 times higher performance in stability but, at roughly the same factor of increased mass, volume and cost. Furthermore the PHM is clearly limited in lifetime due to the size of its Hydrogen reservoir while the RAFS does not have these limitations. This raises the question if it could be favourable to derive an Implicit Ensemble Mean from an ensemble of less stable clocks by composite clock algorithms. By doing this the same stability could be achieved as provided by one highly stable clock while reducing the dependency of the MTR on one individual clock and further allowing a graceful degradation in case of the failure of one or more clocks inside the ensemble.

These different arguments are subject to further studies and the conclusions for the optimum solution may change as also the clocks are evolving. There are ongoing activities to improve RAFS and PHM during the next years. Maybe a sufficient design maturity could be demonstrated also on other clock developments to be flown in space.

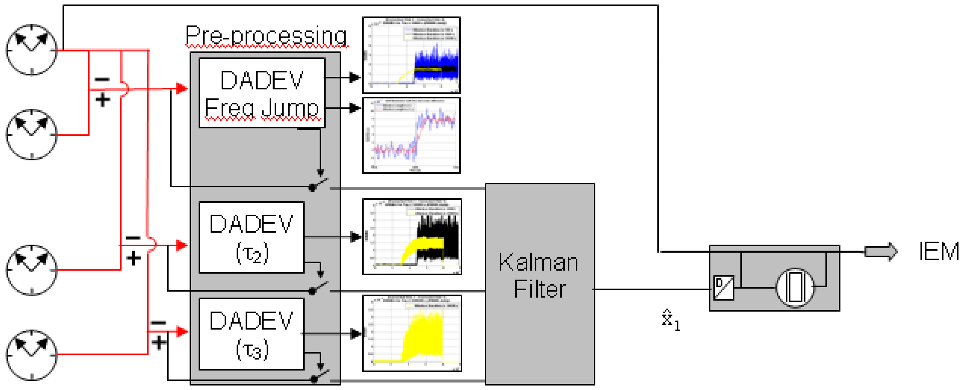

Figure 10. Possible next generation CMCU concept based on composite clock algorithms.

CONCULSION

As shown in this paper, isolation and spectral purity are decisive factors for the performance of a timing subsystem. The necessary isolation requirements were calculated from the required Allan deviation for the MTR based on the occurring phase modulation. To achieve a high spectral purity of the output signal, noise shaping techniques inside the DDS were applied. Based on these insights, a new CMCU concept for Galileo FOC was developed which was optimized to these requirements and can be realized by mainly a re-partitioning of already qualified building blocks
For the next generation of timing subsystems, the implementation of composite clock algorithms was investigated and showed promising results relying on several clocks with moderate performance instead of one high performance clock, to determine the properties of the MTR. However an over-all optimum solution with respect to performance, volume, cost, lifetime and reliability is subject to closer evaluation. This trade-off needs to include the planned improvements on the existing clocks as well as the survey on potential candidates for clocks to be flown in the next generation of Galileo.

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